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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,341	02/09/2004	Hiroaki Jo	118375	6494
25944	7590	03/20/2007	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			NGUYEN, JENNIFER T	
			ART UNIT	PAPER NUMBER
			2629	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	03/20/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,341	JO, HIROAKI	
	Examiner	Art Unit	
	Jennifer T. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 09 February 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-14 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-14 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>2/9/04;3/1/04;8/9/06;10/24/06</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5 and 7-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasai (Patent No. US 6,750,833).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 9, Kasai teaches an electro-optical device (figs. 2, 6, and 14), comprising:

a plurality of scanning lines (Vscan, fig. 6);

a plurality of data lines (Vdata);

a plurality of pixels (1) corresponding to intersections of the scanning lines and the data lines, each of the pixels having a storage device (2) to store data, a driving element (Tr1) to set a driving current flowing from a first power supply line (Vd) to a second power supply line (Vs),

and an electro-optical element (10) to emit light with a brightness in accordance with the set driving current;

a scanning line driving circuit (not shown) to select the scanning line (V_{scan}) corresponding to a pixel in which data is to be written by outputting scanning signals to the scanning lines;

a data line driving circuit (not shown) to output data to the data line (V_{data}) corresponding to the pixel in which data is to be written in cooperation with the scanning line driving circuit; and

a power supply line control circuit (i.e., circuit comprises switch 22) to perform impulse driving of the electro-optical element (10) by setting the electric potential of at least one of the first power supply line (V_d) and the second power supply line (V_s) to be variable and alternately and repeatedly applying a forward bias and a reverse bias to the electro-optical element during a period of time from the moment in which the scanning line corresponding to the pixel in which the data is to be written is selected, to the moment in which the same scanning line is selected again (col. 7, line 16 to col. 8, line 10).

Regarding claims 2-4 and 10-12, Kasai teaches the power supply line control circuit setting the electric potential of the second power supply line ($V_s = GND$) to be lower than the electric potential of the first power supply line ($V_d = V_{cc}$) when a forward bias is applied to the electro-optical element and setting the electric potential of the second power supply line ($V_s = V_{cc}$) to be no less than the electric potential of the first power supply line ($V_d = GND$) when a reverse bias is applied to the electro-optical element (col. 7, line 38 to col. 8, line 10).

Regarding claims 5 and 13, Kasai teaches the power supply line control circuit providing a delayed period of time after the selection of a certain scanning line is stopped until the selection of the next scanning line starts, and performing impulse driving of the electro-optical element during each corresponding delayed period of time (col. 6, line 65 to col. 7, line 5).

Regarding claim 7, Kasai teaches each of the pixels further comprises: a control element (Tr5, fig. 6) provided in the current path of the driving current and the luminescence of the pixel being controlled when data is written by controlling the electrical connection of the corresponding control element (col. 9, lines 26-41).

Regarding claim 8, Kasai teaches a mobile type personal computer equipped with the electro-optical device (fig. 14, col. 10, lines 49-56).

3. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Sanford et al. (Patent No. US 6,734,636).

Regarding claims 1 and 9, Sanford teaches an electro-optical device (figs. 2 and 3), comprising:

a plurality of scanning lines (330, fig. 3);

a plurality of data lines (340, fig. 3);

a plurality of pixels (300) corresponding to intersections of the scanning lines and the data lines, each of the pixels having a storage device (Cs310) to store data, a driving element (Q303) to set a driving current flowing from a first power supply line (Vdd) to a second power supply line (Vss), and an electro-optical element (OLED 320) to emit light with a brightness in accordance with the set driving current;

a scanning line driving circuit (not shown) to select the scanning line (330) corresponding to a pixel in which data is to be written by outputting scanning signals to the scanning lines;

a data line driving circuit (not shown) to output data to the data line (340) corresponding to the pixel in which data is to be written in cooperation with the scanning line driving circuit; and

a power supply line control circuit (325) to perform impulse driving of the electro-optical element (OLED 320) by setting the electric potential of at least one of the first power supply line (Vdd) and the second power supply line (Vss) to be variable and alternately and repeatedly applying a forward bias and a reverse bias to the electro-optical element during a period of time from the moment in which the scanning line corresponding to the pixel in which the data is to be written is selected, to the moment in which the same scanning line is selected again (col. 6, lines 10-67).

Regarding claims 2-4 and 10-12, Sanford teaches the power supply line control circuit setting the electric potential of the second power supply line (Vs = GND) to be lower than the electric potential of the first power supply line (Vd = Vcc) when a forward bias is applied to the electro-optical element and setting the electric potential of the second power supply line (Vs = Vcc) to be no less than the electric potential of the first power supply line (Vd = GND) when a reverse bias is applied to the electro-optical element (col. 6, lines 28-48).

Regarding claims 5 and 13, Sanford teaches the power supply line control circuit providing a delayed period of time after the selection of a certain scanning line is stopped until the selection of the next scanning line starts, and performing impulse driving of the electro-optical element during each corresponding delayed period of time (col. 7, lines 7-20).

Regarding claims 6 and 14, Sanford teaches the power supply line control circuits being provided in units of the scanning lines, and each of the power supply line control circuits performing impulse driving of the electro-optical elements of a row of pixels corresponding to the scanning line in synchronization with the selection of the scanning line corresponding to the corresponding power supply line control circuit (col. 7, lines 22-27).

Regarding claim 7, Kasai teaches each of the pixels further comprises: a control element (Q302, fig. 3) provided in the current path of the driving current and the luminescence of the pixel being controlled when data is written by controlling the electrical connection of the corresponding control element (col. 6, lines 27-40).

Regarding claim 8, Kasai teaches an electronic apparatus equipped with the electro-optical device (col. 1, lines 24-26).

4. The prior art made of record and not relied upon is considered to pertinent applicant's disclosure: Patent. No. US 6,922,182 and Pub. No.: US 2003/0209989.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T. Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

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may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer Nguyen

3/17/07



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